

What Is Claimed Is:

1. A memory circuit having a plurality of sectors having memory cells, comprising:

5 a plurality of blocks, each of which comprises a plurality of regular sectors and a spare sector,

wherein when a regular sector in a first block out of said plurality of blocks is defective, said defective regular sector is replaced with a spare sector in a second
10 block, and

responding to a supplied address, the regular sector corresponding to the supplied address in said first block and the spare sector in the second block are selected simultaneously during a first period, and after said first
15 period, selection of either said regular sector or spare sector, which are simultaneously selected, is maintained according to a result of redundancy judgment on whether the supplied address matches with a redundant address, and selection of the other ends.

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2. The memory circuit according to Claim 1, wherein each one of said sectors further comprises a plurality of word lines respectively, and when a regular sector in said first block and a spare sector in the second block are
25 simultaneously selected responding to said supplied address, the word lines in said regular sector and in the spare sector are simultaneously selected.

3. The memory circuit according to Claim 2, wherein a word line decoder for selecting a word line in a sector is disposed in each one of said sectors, an input signal of said word line decoder is supplied to a first and second blocks at least in said first period, and the word line selection in the regular sector and the word line selection in the spare sector, which are said simultaneous selections, are performed.

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4. The memory circuit according to Claim 2, wherein said simultaneously selected word lines are driven to a first voltage in said first period, and after said first period, the word line of which selection is maintained is driven to a second voltage, which is higher than said first voltage.

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5. The memory circuit according to Claim 4, further comprising a boost circuit for generating a boost power supply which is higher than the power supply,

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wherein said first voltage is power supply voltage level, and said second voltage is boost power supply voltage level, and

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the boost power supply generated by said boost circuit is supplied to the first or second block of which selection is maintained after said first period.

6. The memory circuit according to Claim 1, further

comprising a block select signal generation circuit for
generating a block select signal for selecting said
plurality of blocks,

wherein said block select signal is switched from the
5 first block to the second block when said redundancy
judgment result is a match status after said first period.

7. The memory circuit according to Claim 1,
wherein said plurality of blocks are divided into a
10 plurality of pairs of blocks, and
one of said pair of blocks is said first block and the
other is said second block.

8. The memory circuit according to Claim 1,
15 wherein when the redundancy judgment result is a match,
a spare sector enable signal for selecting said spare sector
and a sector disable signal for disabling selection of said
regular sector are supplied to the respective blocks, and
the spare sector enable signal to be supplied to said
20 second block is enabled so that said spare sector is
selected, in said first period.

9. The memory circuit according to Claim 1,
wherein a Y gate circuit for selecting a bit line in
25 the block is disposed in each one of said blocks, and
said Y gate selects a bit line in the first block when
said redundancy judgment result is a mismatch, and selects a

bit line in the second block when said redundancy judgment result is a match.

10. The memory circuit according to Claim 9,

5 wherein a Y gate select signal to be supplied to said Y gate circuit is driven to a power supply voltage level during said first period, and is driven to a boost power supply voltage level which is higher than said power supply voltage level after said first period, and

10 driving of said Y gate select signal is started according to the redundancy judgment result before said first period ends.

11. The memory circuit according to Claim 1, further being
15 provided with a simultaneous select mode in which sectors of a plurality of blocks are simultaneously selected,

 wherein when said redundancy judgment result is a match status, said simultaneous select mode is disabled.

20 12. The memory circuit according to Claim 1, further being provided with a simultaneous erase mode in which sectors of a plurality of blocks are simultaneously selected and erased,

 wherein when said redundancy judgment result is a match status, said simultaneous erase mode is disabled.

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13. A memory circuit having a plurality of memory cells comprising:

a plurality of blocks, each of which comprises a plurality of regular memory cell areas and a spare memory cell area,

wherein when a regular memory cell area in a first
5 block out of said plurality of blocks is defective, said defective regular memory cell area is replaced with a spare memory cell area in a second block, and

responding to a supplied address, the regular memory cell area corresponding to the supplied address in said
10 first block and the spare memory cell area in the second block are selected simultaneously during a first period, and after said first period, selection of either said regular memory cell area or spare memory cell area, which are simultaneously selected, is maintained according to a result
15 of redundancy judgment on whether the supplied address matches with a redundant address, and selection of the other ends.

14. The memory circuit according to Claim 13, wherein each
20 one of said memory cell areas further comprises a plurality of word lines respectively, and when the regular memory cell area in said first block and the spare memory cell area in the second block are simultaneously selected responding to said supplied address, the word lines in said regular memory
25 cell area and in the spare memory cell area are simultaneously selected.

15. The memory circuit according to Claim 14,

wherein said selected word line is driven to a power supply voltage level during said first period, and after said first period, the word line is driven to a boost power supply level which is higher than said power supply voltage, and

after said first period, said boost power supply is supplied to the word line of which selection is maintained according to said redundancy judgment result.

16. The memory circuit according to Claim 13,

wherein said memory cell area has a plurality of bit lines respectively,

said memory circuit further comprises a Y gate which is disposed in each one of said blocks and selects said bit line, and a Y decoder for supplying a Y gate select signal to said Y gate,

said Y gate select signal is driven to a power supply voltage level during said first period, and is driven to a boost power supply level which is higher than said power supply voltage after said first period, and

after said first period, said boost power supply is supplied to a Y gate select line corresponding to the block of which selection is maintained according to said redundancy judgment result.

17. A memory circuit having a plurality of regular sectors

and spare sectors, comprising:

a redundant memory for storing an address of a defective regular sector; and

a redundancy judgment circuit for comparing a supplied
5 address and the address in said redundant memory,

wherein either said regular sector or said spare sector which is replaced therewith is selected according to a redundancy judgment signal generated by said redundancy judgment circuit, and

10 said redundancy judgment circuit sets said redundancy judgment signal to a match status regardless the address in said redundancy memory so as to enable access to said spare sector responding to a first signal.

15 18. A memory circuit having a plurality of regular sectors and spare sectors, comprising:

a redundant memory for storing an address of a defective regular sector; and

a redundancy judgment circuit for comparing a supplied
20 address and the address in said redundant memory,

wherein either said regular sector or said spare sector which is replaced therewith is selected according to a redundancy judgment signal generated by said redundancy judgment circuit, and

25 said redundancy judgment circuit sets said redundancy judgment signal to a mismatch status regardless the address in said redundancy memory, so as to enable access to the

regular sector which is replaced by said spare sector
responding to a second signal.